UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,434	08/27/2003	Sanjay Dabral	2207/597504	4545

23838 7590 06/23/2006

KENYON & KENYON LLP
1500 K STREET N.W.
SUITE 700
WASHINGTON, DC 20005

EXAMINER	
ZWEIZIG, JEFFERY SHAWN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,434	DABRAL, SANJAY	
	Examiner	Art Unit	
	Jeffrey S. Zweizig	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 5-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 5-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102/103

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5-7 remain rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Houston (USPN 6,429,684).

Fig. 6 discloses a transistor (upper left PMOS transistor) with a gate terminal and body as recited in claim 5. Fig. 6 further discloses a voltage detector (upper right PMOS and NMOS transistors) as recited in claim 5. Fig. 6 further discloses a single source voltage (the supply voltage) supplied to the transistor's body (via the upper right PMOS transistor) and to operate the transistor as recited in claim 5. Claim 5 further requires that the single source voltage be used to couple the transistor's gate terminal voltage. Examiner is interpreting that limitation to mean the supply voltage that supplies

inverter 221 as shown in Applicant's Fig. 2B. Houston Fig. 6 does not specifically show such an inverter, however, such an inverter is believed to be inherent and was merely omitted from Fig. 6 for the sake of clarity. Houston Figs. 5A-5D all show alternate circuit embodiments including an input inverter. The inverter is seen as an implied carry over to Fig. 6 for generating the /IN signal from the IN signal. Furthermore, Figs 4A-4D all show the input inverter receiving the same supply voltage as the rest of the circuit. Again, this is seen as an implied carry over to Fig. 6. In short, the scope and spirit of the Houston reference implies that the circuit of Fig. 6 includes an inverter for coupling the transistor's gate terminal voltage and that that inverter receives the single source voltage as its supply. Thus, Fig. 6 fully anticipates claim 5.

Alternately, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an inverter to Houston Fig. 6 to generate /IN from IN. One of ordinary skill would have been motivated to use an inverter because an inverter has the benefit of being the most common, most straightforward component for generating a complement signal. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to power the inverter from the circuit's existing supply source for the benefit of not having to implement a different supply source when the existing source is perfectly sufficient. Claim 5 is obvious.

The bias voltage (at the body of the transistor) is substantially equal to but slightly less than the terminal voltage due to the voltage drops through the voltage detector as recited in claim 6.

Referring to column 6 it would appear that Houston discloses transistor sizings that would result in the bias voltage being less than the terminal voltage, but not less than the terminal voltage minus a voltage drop across a parasitic diode in the body of the transistor as recited in newly amended claim 7.

Response to Arguments

4. Applicant argues that Houston Fig. 6 does not show a series of two inverters. That is not true. Applicant argues that the IN signal is applied to the upper right PMOS and NMOS transistors. That is also not true. As shown in Fig. 6, /IN is applied to the upper right PMOS and NMOS transistors which are seen as a first inverter. And as explained in the rejection above, a second inverter such as shown in Figs. 5A-5D would be implemented to convert IN to /IN. So there are a series of two inverters coupled from the gate to the body of the upper left PMOS transistor.

The upper right NMOS transistor shown in Houston Fig. 6 is analogous to the NMOS transistor shown in Applicant's inverter 222 (Fig. 2B). Examiner notes that these two transistors have different source configurations. This could be a potential point of distinction, however, such distinction is not seen in claim 5 as presently presented.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey S. Zweizig
Primary Examiner
Art Unit 2816

JZ